PRODUCT FEATURES

SIMULATION
- Mixed VHDL / Verilog Simulation
- Batch Mode Simulation
- Random Stimulus
- Vital optimizations
- Support for VCD and Extended VCD files
- Encryption and Compression

ADVANCED DEBUGGING
- Assertion Support
- Source Code Breakpoints
- Advanced Data Flow
- Waveform Viewer
- Waveform Comparison
- View Event Source
- Signal Agent
- Memory Viewer

CODE COVERAGE
- Coverage per instance & unit
- Toggle Coverage
- Coverage Viewer

USER INTERFACE
- Design Browser
- Design Processor
- HDL Editor
- Library Management
- Library Refresh
- List Window

EXTERNAL INTERFACES
- VHPI Interface
- Verilog PPI and VPI
- Novas - Design
- Verity - Specman
- Design/compile Interface
- Summit Design - Visual Hire
- Synopsys - SWIPT
- SystemC

HARDWARE ACCELERATION
- IPTv2000
- IPTv6000
- IPTv12000

OS PLATFORMS SUPPORTED
- Sun Solaris (7,8 and 9)
- Linux (kernel 2.4)
- Windows NT/2000/XP

SYSTEM REQUIREMENTS
- Sparc or Pentium PC
- 256MB Physical Memory
- Hard Disk Drive with at least 100MB of Free Space (for full installation)

STANDARDS SUPPORT
- VHDL 1076-87/93
- Verilog 1364-95/2001 (partial)
- VITAL 1076.4-95/2000
- SDF 1.0, 2.0 and 3.0
- SystemVerilog (Q1-2004)

Interface
- Tcl/Tk
- PERL
- PLI / VPI
- VHPI
- CHPI

Rev. 04/10/03

The Design Verification Company

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www.aldec.com

- Mixed VHDL / Verilog Simulation
- Co-Simulation for C/C++ and SystemC™
- Advanced Design Debugging
- Assertion-based Verification
- Hardware Acceleration
Riviera is the ultimate performance-driven ASIC design verification solution. The “best-in-class” approach resulted in the most versatile VHDL, Verilog and mixed simulation platform available. Riviera is ideal for RTL debugging, long regression testing, timing simulation, team-based design methodologies and includes direct connection to hardware acceleration with Riviera IPT™.

**MIXED LANGUAGE SIMULATION**
Riviera supports development of the most complex IC designs consisting of VHDL, Verilog, C/C++, SystemC™ and EDIF. Riviera design blocks and provides seamless integration from a common simulation kernel.

**CO-SIMULATION WITH C/C++ AND SYSTEMC™**
New design methods continue to drive decreased verification time. Riviera includes the ability to co-simulate C/C++ and SystemC testbenches and design modules along with VHDL and Verilog. The RTL simulator connects directly to the C compiler and the combined results can be viewed in the Waveform Viewer/Editor.

**OPTIMIZED SIMULATION MODES**
Riviera can be configured to optimize simulation and increased performance in both GUI and batch mode. Performance controls include:
- Optimized Mode - compile and simulate Verilog and mixed VHDL/Verilog designs together with testbenches.
- Sparse Memory Control - selects only the designs memory that is needed during verification.
- Disabled Block Control - disables blocks that are not monitored during simulation.

**ASSERTION-BASED VERIFICATION**
Using Assertion-based Verification in Riviera adds value throughout the process of design, integration, system simulation and tape-out by providing a better (internal) understanding of the design.

**HIGHER DESIGN QUALITY**
Assertion-based verification reduces verification iterations, improves design re-use and outsourcings and can also be utilized in hardware (Riviera-IPT™). Riviera supports development of the most complex IC designs consisting of VHDL, Verilog, C/C++, SystemC™ and includes direct connection to hardware acceleration.

**MEMORY VIEWER**
Riviera simplifies debugging by displaying the content of memories defined in a design for both VHDL and Verilog. The values stored can be observed during simulation.

**CODE COVERAGE**
Coverage tools typically put large overhead on the simulators and slow their run time. Because this feature is built directly into Riviera, the overhead is substantially reduced. Riviera Code Coverage includes:
- Line Coverage (per Instance/Unit)
- Coverage Viewer
- Coverage Merge
- Toggle Coverage

**ADVANCED DEBUGGING TOOLS**
Riviera allows entering and debugging VHDL, Verilog and mixed design and performing source code debugging online or post simulation using several advanced features that give designers total control over the source code and speeds design debugging.

**RIVIERA-IPT HARDWARE ACCELERATION**
Riviera can be upgraded with an optional patented hardware accelerator Riviera-IPT, which provides greater speed and efficiency by bringing together development design and verification elements on one seamless accelerated system-level platform. This platform combines software simulation for mixed VHDL, Verilog, assertions, C/C++, SystemC co-simulation and hardware acceleration all optimized and connected to the common kernel architecture. Key features include:
- 10X-50X RTL Acceleration
- Scalable Architecture
- No Learning Curve or Set-up Time
- Network and Team-Based Operation
- Higher Design Quality
- Supports Server Farm Methodology

**OBJECT-ORIENTED DESIGN**
Traditional simulation methodologies require users to re-simulate previously proven HDL blocks with each newly added block or design iteration, making verification slow and inefficient. However, since Incremental Prototyping Technology “pushes” all verified blocks into hardware, Riviera-IPT only simulates the newly added HDL blocks in software, dramatically accelerating the simulation process.

**PRODUCT SUPPORT**
Aldec provides the highest level of customer support in the industry. Annual product maintenance includes unlimited technical support around the globe, quarterly product releases and updates, subscription to our newsletter and newsgroups including access to our on-line support library.

IEEE INTERFACES
Riviera includes IEEE standard PLI, VPI and VHPI interfaces for connection to other verification tools in the design flow. In addition to the standard interface, Riviera also includes optimized integration to select strategic partner tools.

SERVER FARM SUPPORT
Riviera is compatible with all server farm load management methodologies configured for UNIX, Linux or NT operating systems. Designs can be offloaded from local workstations or a PC to a central location, freeing the local machine to work on other parts of the design.

LIBRARY ENCRYPTION
Riviera provides source compression and encryption for VHDL and Verilog to safely pack and distribute designs among team members locally or over the network.

CODE VIEWER
The Waveform Viewer/Editor is integrated with the compiler and simulator to simplify debugging, enabling breakpoint settings and for quick location of compilation errors.

**ADVANCED DATAFLOW**
The Advanced Dataflow offers the ability to view and debug the design graphically and is useful for exploring the physical connectivity of the design for both VHDL and Verilog. It connects directly to Riviera’s stand-alone Waveform Viewer and uses the cursor to scroll back and forth through simulation while observing the annotated values in the diagram.

**NEW DESIGN METHODS CONTINUE TO DRIVE DECREASED VERIFICATION TIME**
Riviera includes IEEE standard PLI, VPI and VHPI interfaces for connection to other verification tools in the design flow. In addition to the standard interface, Riviera also includes optimized integration to select strategic partner tools.
Riviera is the ultimate performance-driven ASIC design verification solution. The “best-in-class” approach resulted in the most versatile VHDL, Verilog and mixed simulation platform available. Riviera is ideal for RTL debugging, long regression testing, timing simulation, team-based design methodologies and includes direct connection to hardware acceleration with Riviera IPT™.

**MIXED LANGUAGE SIMULATION**

Riviera supports development of the most complex IC designs consisting of VHDL, Verilog, C/C++, SystemC™ and EDIF. Netlist design blocks and provides seamless integration from a common simulation kernel.

**CO-SIMULATION WITH C/C++ AND SYSTEMC™**

New design methods continue to drive decreased verification time. Riviera includes the ability to co-simulate C/C++ and SystemC™ testbenches and design modules along with VHDL and Verilog. The RTL simulator connects directly to the C compiler and the combined results can be viewed in the Waveform Viewer/Editor.

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**ASSERTION-BASED VERIFICATION**

Using Assertion-based Verification in Riviera adds value throughout the process of design, integration, system simulation and testing. By providing a better (internal) understanding of the design, Assertions speed debugging by reducing verification iterations, improve design re-use and outsourcing and can also be utilized in hardware (Riviera-IPT™). Assertion standard support includes:

- OpenVera™ Assertions (OVA)
- Property Specific Language (PSL)
- Open Verification Libraries (OVL)

**HIGH PERFORMANCE WAVEFORM VIEWER AND EDITOR**

The Waveform Viewer uses several compression techniques for handling large simulation data and speeding the Waveform Viewer display. In addition to performance the Waveform Viewer/Editor also includes several features that simplify design verification, allowing faster and more accurate editing and analysis of simulation data. Editing features include the ability to modify values and nets, which can then be applied to subsequent simulation runs. Additional features include:

- VCD & Extended VCD Support
- Show Event Source
- Waveform Comparison
- Stimulator Management
- List Viewer (Latex)

**IEEE INTERFACES**

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**ADVANCED DEBUGGING TOOLS**

Riviera allows entering and debugging VHDL, Verilog and mixed and performing source code debugging online or post simulation using several advanced features that give designers total control over the source code and speeds design debugging.

**SIGNAL AGENT (VHDL ONLY)**

Signal Agent allows a designer to monitor and drive signals from any VHDL block. Signals do not have to be routed via the interface or declared in global packages. This is particularly useful in testbench development and design verification.

**MEMORY VIEWER**

Riviera simplifies debugging by displaying the content of memories defined in a design for both VHDL and Verilog. The values stored can be observed during simulation.

**X-TRACE**

X-Trace allows the designer to trace and view events that cause unexpected output values during simulation. It is accessed through the Advanced Dataflow window in conjunction with the Waveform Viewer. Using X-Trace will dramatically reduce overall debug time.

**ADVANCED DATAFLOW**

The Advanced Dataflow offers the ability to view and debug the design graphically and is useful for exploring the physical connectivity of the design for both VHDL and Verilog. It connects directly to Riviera’s stand-alone Waveform Viewer and uses the cursor to scroll back and forth through simulation while observing the annotated values in the diagram.

**DESIGN PROFILER**

Design blocks that consume more simulation runtime can be easily identified using the Design Profiler. By identifying these blocks and focusing on areas that are increasing simulation time the overall design simulation can be significantly decreased. Without the ability to see the design characteristics and identify simulation degradation, simulation can be highly inefficient.

**POWERFUL HDL EDITOR**

The HDL editor is integrated with the compiler and simulator to simplify debugging, enabling breakpoint settings and for quick location of compilation errors.

**RIVIERA-IPT HARDWARE ACCELERATION**

Riviera can be upgraded with an optional patented hardware accelerator Riviera IPT, which provides greater speed and efficiency by bringing together and design and verification elements on one seamless accelerated system-level platform. This platform combines software simulation for mixed VHDL, Verilog, assertions, C/C++, SystemC™ co-simulation and hardware acceleration all optimized and connected to the common kernel architecture. Key features include:

- 10X-50X RTL Acceleration
- Scalable Architecture
- No Learning Curve or Set-up Time
- High Design Quality
- Supports Server Farm Methodology

**RIVIERA-IPT METHODOLOGY**

Traditional simulation methodologies require users to re-simulate previously proven HDL blocks with each newly added block or design iteration, making verification slow and inefficient. However, since Incremental Prototyping Technology “pushes” all verified blocks into hardware, Riviera-IPT only simulates the newly added HDL blocks in software, dramatically accelerating the simulation process.

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**PRODUCT FEATURES**

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**OS PLATFORMS SUPPORTED**
- Sun Solaris (7, 8 and 9)
- Linux (kernel 2.4)
- Windows NT/2000/XP
- Sparc or Pentium PC Compatible Computer
- 256MB Physical Memory
- Hard Disk Drive with at least 100MB of Free Space (for full installation)

**SYSTEM REQUIREMENTS**
- Sparc or Pentium PC Compatible Computer
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**INTERFACE**
- Tcl/Tk
- PERL
- PLI / VPI
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**WEB SITE**
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