

SYNPLICITY'S SYNPLIFY SYNTHESIS

Active-HDL with Synplify is a complete FPGA design entry, simulation and synthesis solution. Working in conjunction with Synplicity's powerful Synplify synthesis tool, Active-HDL with Synplify offers system designers the ability to support mixed VHDL, Verilog and EDIF designs. The seamless environment is optimal for supporting the highest density FPGA designs.

Seamless Integration

Active-HDL's Design Flow Manager allows for push button initialization of the Synplify software and all files generated by the logic synthesis software are back annotated directly into Active-HDL. The automation increases overall design productivity and offers a single entry, synthesis and verification solution for all CPLD and FPGA vendors.

Project Management

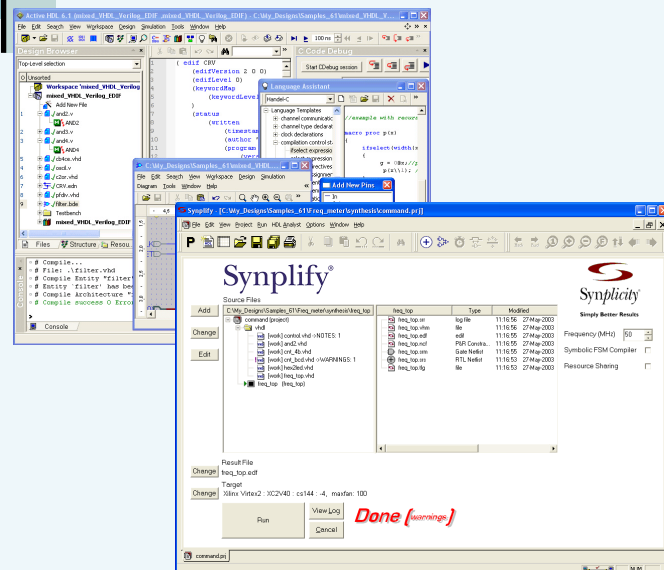
The Design Flow Manager is an effective project management tool to control all stages of the design process from design entry through logic simulation and synthesis. All software elements are controlled through the graphical Design Flow Manager, which allows the selection of simulation, synthesis and place and route settings, and viewing reports and cross-probe error messages.

Synplify Synthesis

Synplify is a high-performance logic synthesis engine that delivers fast, highly efficient FPGA and CPLD designs. Synplify takes Verilog and VHDL Hardware Description Languages as inputs and outputs an optimized netlist in the most popular FPGA vendor formats.

Job Control Software (JCS)

Aldec's Job Control Software provides direct control of team-based designs in a networked environment. JCS allows fast and efficient management of team-based designs directly from the Active-HDL software application. Designed specifically for Active-HDL, JCS also offloads processor dependent application such as simulation, Synplify's synthesis and place and route to a remote computer and returns the results.



Mixed VHDL, Verilog and EDIF Design

As the amount of designs using mixed languages and IP Cores escalates, the demand for flexible tools becomes increasingly more important. The ability to freely mix IP cores with VHDL, Verilog and EDIF during the design process makes the combination of Active-HDL and Synplify software an extremely versatile tool for today's design requirements. The ability to reuse old designs as new blocks for a current design shortens the development process, helping to move products to market faster.

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