

# Choose Your Destination

## Emulation

10 MHz

## Acceleration

500 KHz



## Hardware Emulation System

**HES™** is a versatile emulation and acceleration solution for large complex ASIC and SOC designs which require millions of simulation cycles. The strength of the tool is in automatic design compilation, standard testing interface, integration with industry leading hardware/software debugging tools and the power to transform your existing ASIC prototyping into dynamic emulation.

### Top Features

- SOC (ASIC and FPGA)
- Functional RTL acceleration
- Emulation at 10MHz (TLM)
- Transaction Level interface (SCE-MI 2.0 and SystemC, C/C++)
- Internal Debugging
- DINI and HAPS hardware support

### Hardware Assisted Verification

HES provides no-hassle ASIC and FPGA design compilation to the hardware with automatic design partitioning, clock domain conversion, memory mapping and many other techniques. HES can target a commercial off-the-shelf prototyping platform such as The DINI Group and Synplicity®/Synopsys® HAPS™ for hardware emulation and acceleration.

### Emulation

HES provides functional verification of an entire design in a multi FPGA platform. The design is exercised using real data, flowing through transaction level interface such as the industry standard SCE-MI interface or C/SystemC API. Built-in debugging tools allows for quick localization and capturing bugs quickly. Additionally, HES supports interfaces to Novas® Siloti™ and Verdi™ for RTL annotated debugging.

### Acceleration

Another application of HES is acceleration of functional simulation. HES interfaces to popular industry-leading RTL simulators from Aldec, Synopsys®, Cadence® and MentorGraphics®. The design is off-loaded to the hardware and exercised by the HDL test bench running in the HDL simulator.



**STANDARDS**



**PARTNERS**



**INTERFACES**



**FEATURES**

**PRODUCT CONFIGURATIONS**

Software Features	Xcell	Elite
Design Verification Manager (DVM™)	•	•
Daughterboard Connection (connection to external boards and/or devices)	•	•
Super Macro support (groups modules together for increased performance)	•	•
Manual Design Partitioning (manual mapping based on resource information)	•	•
Automatic Design Partitioning—with signal multiplexing using LVDS		•
Mixed Partitioning—manual mapping of modules, whole design is automatically partitioned	•	•
Blackbox Functionality (excludes modules from acceleration)	•	•
Testbench Optimizer—VHDL to C++ Conversion	•	•
Device Debugging (debug of internal hardware signals in simulator)	•	•
Clock Conversion and Analysis (convert multiple clock domains to one)	•	•
Memory Model Mapping (maps user memory to on-board memory)	•	•
Prototyping API and function library (interface with C++ domain)		•
Interface to Xilinx® ChipScope™ Pro (device debugging)		•
Emulation Mode (design clock up to 10 MHz)		•
Emulation Results Stored in Waveform (ASDB and VCD)		•
Memory Model Viewer	•	•
Emulation Debugging		•
SCE-MI 2.0 interface support		•
Multi-Chip Design Access (ability to use multi-chip FPGA boards)	Single Only	•
Interface to Hardware Boards—includes drivers (Aldec®, Synplicity® HAPS™ or The Dini Group)	Choice of One	Choice of One
HDL Simulator Interface (Aldec®, Cadence®, Mentor® or Synopsys®)	Choice of One	Choice of One
<b>Additional Software Options</b>		
Additional HDL Simulator Interface (Aldec®, Cadence®, Mentor® or Synopsys®)	Option	Option
Additional Interface to 3rd Party Hardware Boards—includes drivers and daughter card to support additional boards (Synplicity® HAPS™ or The Dini Group)	Option	Option
<b>Hardware Boards</b>		
<b>Single Chip FPGA Boards (FPGA Acceleration and Prototyping)</b>		
Virtex™-II FPGA—up to 1 million Xilinx® FPGA gates (Single V2-1000 Chip)		Aldec
Virtex™-II FPGA—up to 3 million Xilinx® FPGA gates and 1 GB SDRAM (Single V2-3000 Chip)		Aldec
Virtex™-II FPGA—up to 6 million Xilinx® FPGA gates and 128 Mb RAM (Single V2-6000 Chip)		Aldec
Stratix™-I FPGA—up to 30,000 Altera® Logic Elements and 1 GB RAM (Single S25EX Chip)		Aldec
Stratix™-I FPGA—up to 90,000 Altera® Logic Elements and 1 GB RAM (Single S80EX Chip)		Aldec
<b>Multi-Chip FPGA Boards (ASIC Acceleration/Emulation and Prototyping)</b>		
Virtex™-II FPGA—up to 1 million ASIC gates and 256 Mb RAM (Dual V2-6000 Chips)		Aldec
Virtex™-4 FPGA—up to 2 million ASIC gates and 1 GB DDR2 (Dual, V4LX200 Chips)		Aldec
Virtex™-4 HAPS-34—3–6 million ASIC gates (4–Xilinx® Virtex-4 Chips, either LX100, LX160 or LX200)		Synplicity/Synopsys
Virtex™-5 DN—up to 4 million ASIC gates and DDR2 (Dual, V5LX330 Chips)		The Dini Group
Virtex™-5 HAPS-54—8 million ASIC gates (4–Xilinx® Virtex-5 LX330 Chips)		Synplicity/Synopsys
Virtex™-5 DN—up to 10 million ASIC gates and DDR2 (6–V5LX330 Chips)		The Dini Group
Virtex™-5 DN—up to 32 million ASIC gates and DDR2 (16–V5LX330 Chips)		The Dini Group
<b>Computer Platforms</b>		
Supported Operating Systems: Linux® 32/64, Windows® 2000/2003/XP/Vista		

Technology Patent no. 5,479,355; System and method for a closed loop operation of schematic designs with electrical hardware  
Technology Patent no. 7,003,746; Method and apparatus for accelerating the verification of application specific integrated circuit designs



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