

# DO-254 Compliance

**Aldec DO-254 CTS** (Compliance Tool Set) provides support for the "Design Assurance Guidance for Airborne Electronic Hardware" (DO-254/ED80) chapter 6.2 "Verification Process" and chapter 11.4 "Tool Assessment and Qualification Process". Aldec provides a fast and reliable verification process for assurance levels A, B, C and D with a focus on increased testability in hardware together with design requirements traceability.

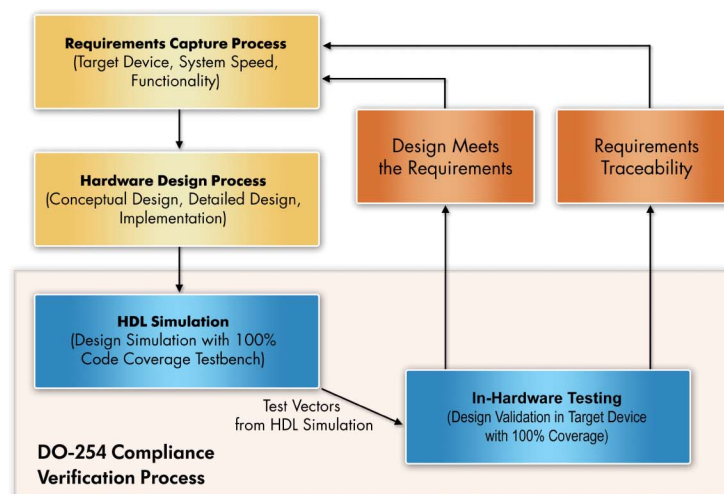
## Top Features

- Design verification in the target device
- In-hardware verification performed at speed
- Same number of tests run in the target device as in the simulator with 100% functional coverage assured
- Automated output waveform comparison between the HDL simulation and in-hardware testing results
- Technology Patent no. 5,479,355; System and method for a closed loop operation of schematic designs with electrical hardware

## Aldec's DO-254 CTS Configuration

Aldec DO-254 CTS consists of two elements: HDL Simulation and an in-hardware simulation system that supports the customer's specific target device. The in-hardware testing system includes: Windows®, Linux® or Solaris® Workstation (32 bit/64 bit); Aldec mixed language common kernel software simulator (Verilog®, System Verilog, Assertions, VHDL, SystemC, C/C++ and EDIF); Compliance

Verification Tool (CVT) Software; PCI/PCIe main board and custom daughter board containing the target FPGA device.



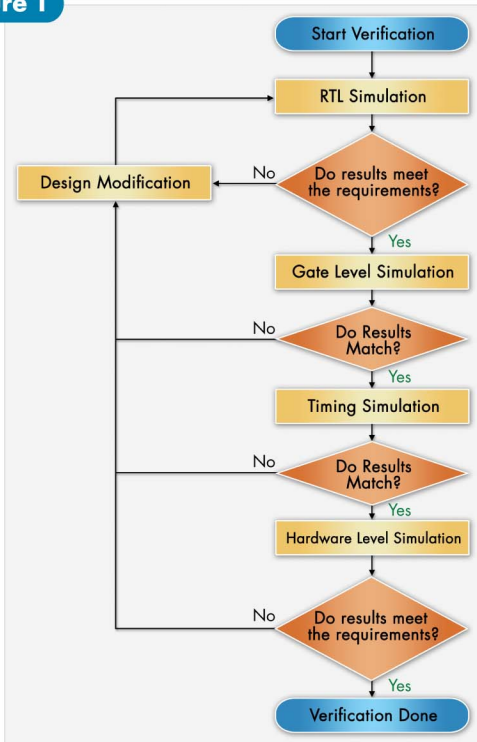
## HDL Simulation Tool Suite

Aldec's HDL Simulation Tool Suite provides HDL simulation (source level), post-synthesis simulation (gate level) and post place-and-route simulation (timing level), all performed in one software environment. The tool suite combines code linting, code coverage, profiling, automated documentation and waveform comparison tools to enhance verification productivity. The simulator uses the designer-created testbench to verify the design functionality and provides coverage metrics to measure how effectively the testbench has exercised the design. The simulation results are stored in the waveform format and automatically compared to the results from the different stages of simulation.

# Methodology Diagram

Aldec DO-254 CTS methodology consists of four levels of verification as seen in Figure 1 below.

**Figure 1**



The HDL simulation testbench is automatically converted to a set of test vectors by the Aldec software. The vectors are then written into the memory buffers on the PCI main board. The test vectors are fed from the PCI main board to the target FPGA (or PLD, ASIC) device, located on the custom daughter board. The Aldec software then reads the output vectors back from the target FPGA and converts them to the waveform format for display in the Aldec simulator with the waveform viewer. The design functionality is considered proven if the output waveforms captured from in-hardware simulation match the waveforms generated during HDL simulation.

## Assuring Compliance with At-Speed Verification

Aldec DO-254 CTS provides assurance that the hardware item implementation meets the compliance requirements. In the verification flow, testing requirements are checked first in the HDL simulator and later in the target hardware. Traditionally, when a design is tested in the hardware it lacks the testability and traceability available with HDL simulation, where the designer can drive or probe any signal. Since it is not always possible or easy to check all of the test scenarios in the hardware, typically only major design functions are verified. Additional analysis is then required to prove the coverage of the lower level requirements. Aldec DO-254 CTS bridges this gap in the DO-254 verification process. The same testbench with 100% functional coverage from HDL simulation is used to test the design in the target device. All of the output waveforms captured from the target device during in-hardware simulation are saved and automatically compared to the output waveforms from the earlier HDL simulation. These in-hardware output waveforms are automatically documented to provide traceability with the design test requirements. In addition, in-hardware simulation independently assesses the outputs of the synthesis, place-and-route and simulation tools, fulfilling the DO-254 requirements for tool assessment and qualification of these tools.

## In-Hardware Simulation

To begin in-hardware simulation, the designer needs to create the target FPGA (or PLD) bit-file. Next, the bit-file will be downloaded to the target device on the daughter board. After this hardware setup, the Aldec simulator can be initialized for in-hardware simulation using the HDL simulation testbench (see Figure 2).

**Figure 2**

Aldec Simulator and CVT Software

