

FPGA Designs Made Easy

- Performance
- Unity
- Control



Active-HDL

Active-HDL™ is a completely integrated FPGA design and verification solution, providing ease-of-use, advanced verification and debugging capabilities for today's most complex FPGA designs. A multi-vendor FPGA flow manager controls simulation, synthesis and implementation for all devices from Actel®, Altera®, Lattice®, Quicklogic®, Xilinx® and other FPGA vendors.

Top Features

- Graphical design entry including FPGA vendor primitives
- Mixed language HDL simulation
- Pre-compiled FPGA vendor libraries
- Automatic testbench generation
- Import legacy designs
- Code2Graphics and Graphics2Code
- DSP design and co-simulation with MATLAB®/Simulink®
- HTML and PDF design documentation
- Code coverage analysis and Linting
- Open IP Encryption

Intuitive Design Entry Tools

You can learn new languages as you design, with the built-in language assistant for VHDL, Verilog®, SystemVerilog and SystemC that provides pre-defined templates, embedded language reference manuals and type-ahead command completion. Draw powerful finite state machine diagrams and let the tool generate your synthesizable RTL code. Quickly connect all design modules at the top-level and output structural HDL using the built-in block diagram editor. Code2Graphics tools allow you to easily visualize designs imported from VHDL, SystemVerilog or Verilog.



High Performance, Mixed Language Simulation

Active-HDL includes a high performance, common-kernel, mixed language simulator supporting Verilog, SystemVerilog, VHDL, VITAL, SDF, EDIF and SystemC on a Windows-based 32/64 bit platform. Drive your system-level simulation model using complex testbenches or create quick and flexible stimulators to rapidly test design modules. Co-simulate MATLAB functional DSP blocks with HDL models in a high-level mathematical modeling environment.

Debugging Made Easy

Active-HDL provides highly intuitive, graphical debugging tools including a high performance waveform viewer/editor and graphical dataflow for quickly tracing signal drivers/readers across multiple levels of design hierarchy and unknown values to their origin.

Code Coverage Analysis and Linting

A powerful HDL code coverage analyzer helps achieve 100% test coverage of all RTL statements, lines, signals and logical expressions in the design. An embedded Lint tool checks for reliable, predictable and portable HDL code.

Team Based Design Management

Increasing design size and complexity requires a team based approach for many projects. Active-HDL links to most source code revision control software, has a built-in server farm manager to automate regression testing and provides multi-design workspaces to enable collaboration. Produce finish-quality, system-level documentation in HTML and PDF with hierarchical hot-links.



STANDARDS



SILICON



INTERFACES



FEATURES

PRODUCT CONFIGURATIONS

	DM	DE	PE	EE
Project Management				
Support for Multi-Design Workspace	•	Single Design Support	•	•
Design Flow Manager for All FPGA Vendors	•	•	•	•
Revision Control Interface	•	•	•	•
Design Entry				
HDL, Text, Block Diagram and State Machine Editor	•	•	•	•
Language Assistant with Templates and Auto-Complete	•	•	•	•
Code2Graphics™ Converter	•	•	•	•
Macro, Tcl/Tk, Perl script Support	•	•	•	•
Pre-Compiled FPGA Vendor Libraries	•	•	•	•
Legacy Schematic Design Import and Symbol Import/Export	•	•	•	•
Code Generation Tools				
Testbench Generation from Waveform		•	•	•
Testbench Generation from State Diagram			•	•
IP Core Component Generator	•		•	•
Simulation/Verification				
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)		•	•	•
Verilog® HDL IEEE 1364 (1995, 2001 and 2005)		•	•	•
SystemC™ 2.2 IEEE 1666/OSCI 2.2			Option	•
System Verilog IEEE 1800 (Design)		•	•	•
EDIF 2.0.0		•	•	•
PSL IEEE 1850 Assertions and Coverage				Option
SystemVerilog IEEE 1800 (Assertions) and Coverage				Option
OpenVera Assertions and Coverage				Option
Single or Mixed Language		•	•	•
Verilog HDL Simulation Acceleration			Option	•
Simulation Model Protection/Library Encryption		•	•	•
Debug and Analysis				
Code Execution Tracing		•	•	•
Advanced Breakpoint Management		•	•	•
Standard Waveform Editor and List Viewer (AWF)	Viewer Only	•	•	•
Accelerated Waveform and List Viewer (ASDB)			•	•
Waveform Compare and Memory Viewer			•	•
Post Simulation Debug Mode			•	•
C++ Debugger			•	•
Advanced Dataflow		Option	Option	•
XTrace, Profiler and Signal Agent			Option	•
Basic Lint (VHDL and Verilog)			Option	•
External Simulation Interface				
Synopsys® SmartModels®, SWIFT™ Interface and LMTV		Option	Option	•
Novas® FSDB Writer		Option	Option	•
Denali® Memory Model Interface (VHDL and Verilog)		Option	Option	•
Coverage Tools				
Statement, Branch and Expression Coverage		Option	Option	•
Toggle Coverage		Option	Option	•
Co-Simulation				
Simulink® Co-Simulation		Option	•	•
MATLAB® Co-Simulation		Option	Option	•
Documentation				
Export to PDF/HTML/Bitmap Graphics	•		•	•
Advanced Export to PDF (Vector Graphics)	Option		Option	•
Computer Platforms				
Supported Operating Systems: Microsoft®Windows® 2000/2003/XP/Vista				

Technology Patent no. 5,051,938; Simulation of selected logic circuit designs



2260 Corporate Circle Henderson, Nevada 89074 • Phone: 702.990.4400 • Fax: 702.990.4414
Copyright © 2008, Active-HDL is a trademark of Aldec, Inc. All other trademarks or registered trademarks are property of their respective owners.



2, Rue Galilée – 78280 GUYANCOURT – Tél. 01.39.30.65.06 – Fax. 01.39.30.65.08

www.cadvision.fr

R4_08